Radiation Hard SiC Microprocessor

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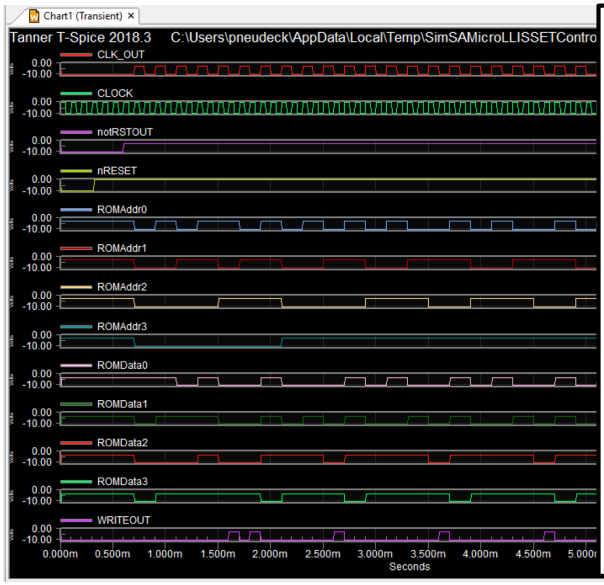
Target: Design, build, and test rad-hard microprocessor based upon SiC Junction Field Effect Transistors (JFETs). Goal of 7 Mrad TID and single-event LET 86 MeV-cm^2 (achieved for simpler SiC integrated circuits[1]) could eliminate significant radiation shielding mass for Europa and other longer-duration gas-giant missions.

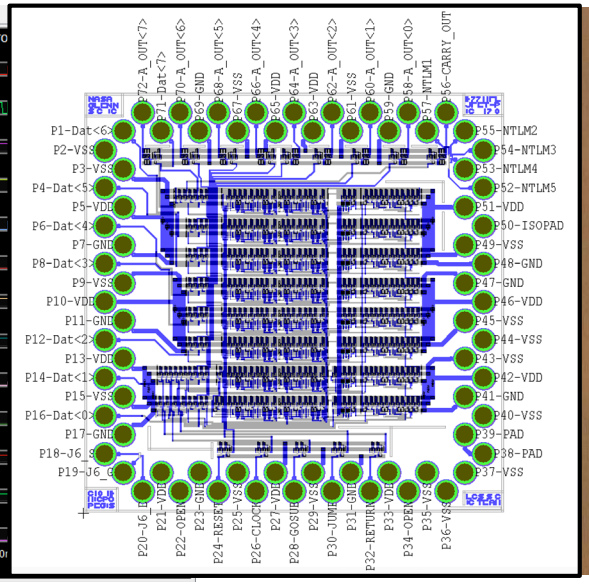
Milestone Update:

- SiC "one-bit microprocessor" (OBµP) circuit design completed, spans two SiC IC Version 12 chips.
- Design verified using SPICE transient simulations. Runs instruction set & integrates with SiC memory.
- SiC chips about halfway through fabrication, but progress frozen by COVID-19 mandatory telework.
- Telework focusing on designing circuit boards, instrumentation, and programming for radiation testing.

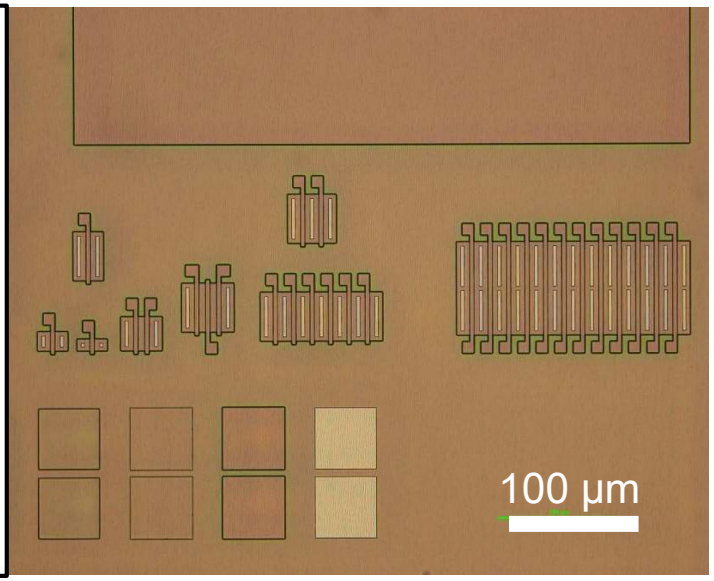
SiC OBµP Simulation Waveforms
(Running program from SiC ROM)



SiC OBµP Chip#1 Layout
(5 mm x 5 mm, 964 SiC JFETs)



SiC IC Version 12 JFETs in Fabrication
(Need interconnects added to become ICs)



Issues: Estimate ~1 year after return to onsite work from COVID under current conditions and with present resources to: 1. Restore GRC fabrication lab (accumulating maintenance & repairs backlog) and 2. Finish construction of IC Version 12 chips.

1. J. Lauenstein et al., 2019 IEEE Radation Effects Data Workshop, https://ntrs.nasa.gov/citations/20190031951