Prioritized Technology: High performance/low power/rad hard computing and FPGAs

Capability Description

High Performance Space Computing (HPSC) consists of the development of a chiplet, memory, co-processors and accelerators, system software, a development environment, power, and a computer prototype. Capability advancements needed include:

- Fault-tolerant real-time processing, high efficiency cache execution, space wire and serial I/O compatibility

Radiation-hardened components are needed:

- Digital signal processor, graphics and machine vision processors, neuromorphic deep learning/recognition engine, single A53 core embedded processor, high performance Field Programmable Gate Array.

Space-qualification is needed:

- Real-time operating system, common flight software package for standard s/c avionics, configuration middleware, parallel processing middleware, and parallel and serial math packages.

A development environment is need for state-based compilers, and both static and dynamic analysis validation and verification.

Mission Applications

- Virtually all NASA space missions would benefit from application of the Chiplet:
  - Low SWaP-C for small/low complexity spacecraft
  - High Performance at low power for larger more complex spacecraft
  - Onboard science data processing to overcome low bandwidth downlink
  - Autonomy for improved productivity and increased science return/$
  - Improved fault tolerance and spacecraft life through evolvable distributed computing

- Most NASA space missions would benefit from application of these memories:
  - HPSC-based s/c - improved radiation hardness at COTS-like performance for working memory
  - Non-HPSC-based s/c - improved performance and radiation hardness for generic processors and FPGA-based applications
  - Instrument processors – improved performance at significantly reduced SWAP-C
  - Missions requiring large mass store capabilities – high capacity, high speed, non-volatile memory
  - Digital signal processor - RADAR, HSI, LIDAR other digital signal processing intensive sensor systems
  - Vision – robotic autonomous exploration and science missions
  - Neuromorphic – robotic autonomous exploration and science missions
  - U-Chiplet (micro-Chiplet) – virtually all missions either as main processor for small-sats or as subsystem/instrument-embedded processor
  - FPGA – virtually all missions – multiple uses
  - Virtually all s/c will require an RTOS and CFE/CFS. Most HPSC-based missions will also require configuration middleware to simplify HPSC management. Many missions will also need significant parallel processing for onboard science data processing, autonomy processing and robotics processing – these will require parallel processing middleware and math libraries. Note: The two primary flight software packages are CFE and CFS from GSFC and JPL respectively – it is assumed that each center will port an initial version of its package to HPSC.
  - All missions will benefit from static analysis of software –most are currently using some form of this today. State based compilers and dynamic analysis will benefit all missions due to improved reliability, fault tolerance and correct-code generation capabilities.

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<thead>
<tr>
<th>Volatile Chip (VC)</th>
<th>300krad, DDR3/4, 1Gb</th>
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<tr>
<td>Non- Volatile Chip (NVC)</td>
<td>300krad, DDR3/4, 4Gb</td>
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<tr>
<td>Volatile Stack (VS)</td>
<td>300krad, Serial I/O, 8+Gb</td>
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<tr>
<td>Non-Volatile Stack (NVS)</td>
<td>300krad, Serial I/O, 32+Gb</td>
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